Amendments to the Specification:

Please replace the paragraph extending from page 1, line 25 to page 2, line 5, with the following amended paragraph:

During emulation, test stimuli are either generated on the workstation or on a service board of the emulation system under the control of the workstation, and then transferred to the various logic boards for input into the emulation ICs for application to the various netlists of the IC design being emulated. State data of various circuit elements as well as signal states of interest of the IC design being emulated, would be correspondingly read out of the applicable FPGAs, and then transferred off the logic boards, for analysis on the workstation.

Please replace the paragraph at page 3, lines 9-14, with the following amended paragraph:

In one embodiment, the distributed data processing resources are disposed on logic boards of an emulation system. In other embodiments, at least some of the distributed data processing resources are disposed on the emulation ICs of the logic boards. The board and IC disposed ~~distribtued~~ distributed processing resources cooperatively perform the earlier mentioned distributed and corresponding monitoring and reporting of events, and generation and application of testing stimuli.

Please replace the paragraph at page 7, lines 3-8, with the following amended paragraph:

Emulation ICs **104,** in particular, their on-chip reconfigurable logic and interconnect resources, as in prior art "FPGAs", are used to "realize" the netlists of an IC design to be emulated. In various embodiments, each emulation IC **104** may advantageously include integrated debugging facilities, such as those included with enhanced "FPGAs" described in USP 5,777,489, and co-pending U.S. Patent Application number ~~<insert the CIP number here>~~09/404,925, now U.S. Patent No. 6,265,894, to be described more fully below.

Please replace the paragraph beginning at page 9, line 13 and extending to at page 10, line 2, with the following amended paragraph:

Referring now to **Figures 2a-2b,** wherein two block diagrams illustrating an emulation IC **104** in further details, in accordance with one embodiment, are shown. As illustrated in **Fig. 2a,** emulation IC **104** includes reconfigurable LEs (RLR) **202,** reconfigurable interconnects (RIN) **204,** emulation memory (MEM) **206,** debugging resources (DBR) **208,** context or state elements (CTX) **210,** and configuration registers (CR) **212** and **214** coupled to each other as shown. Reconfigurable LEs **202,** emulation memory **206** and context/state elements **210** are used to "realize" circuit elements of the netlists of an assigned partition of an IC design to be emulated. In particular, reconfigurable LEs **202** are used to "realize" the combinatorial logic of the netlists of the assigned partition of an IC design to be emulated. Context/state elements **210** are used to "realize" state elements of the ~~netliest~~ netlist of the assigned partition of the IC design to be emulated, such as flip-flops, and so forth, whereas emulation memory **206** are used to "realize" storage elements of the netlists of the assigned partition of the IC design to be emulated.

Reconfigurable interconnects **204** are used to ~~reconfigurbaly~~ reconfigurably couple LEs **202**, memory 206 and so forth.

Please replace the paragraph at page 10, lines 3-9, with the following amended paragraph:

In various embodiments, configuration of these elements, including determination of the interconnect routing, to emulate the netlists of an assigned partition of an IC design, reading of state data of state elements, including determination of which state elements to read, capturing of signal states, including recreation of "unobservable" signals, are locally (i.e. distributively) performed by data processing resources **102** of the host logic board **100**, to be described more fully below.

Please replace the paragraph extending from page 11, line 22 to page 12, line 11, with the following amended paragraph:

Figure 4 illustrates an overview of the software modules provided to data processing resources **102** to provide the desire functionalities of the present invention to a logic board, in accordance with one embodiment. As illustrated, software **400** includes control module **402**, and functional modules, router **403**, configurator **404**, trace data processor **406**, state data/event detector **408**, and test stimuli generator **410**. Control module ~~602~~ 402 is equipped with control logic to facilitate the overall operation in the delivery of the desired functions, including in particular communication with external entities outside a logic board **100**, and invocation of appropriate ones of the functional modules. In one embodiment, control module **402**

communicates with the external entities on a request and response transaction basis, via communication packets. That is, under the present invention, the assigned netlists, as well as the routing, configuration, signal state, state data of state elements, and testing requests are made, acknowledged and responded to using transaction messages sent and received in a series of communication packets. Of course, in alternate embodiments, other communication techniques may be used instead.

Please replace the paragraph at page 13, lines 17-25, with the following amended paragraph:

Trace data processor **406** is equipped with logic to locally pre-processes the captured signal states of the emulation signals to determine one or more signal states of one or more signals of interest of the netlists of the assigned partition of the IC design being emulated, responsive to trace data requests. Again, except for the fact that the captured signal states of the emulation signals are pre-processed locally, reconfiguration of debugging resources and processing of capture signal states, in and of themselves, are otherwise substantially the same as these tasks are centrally performed on a control workstation of an emulation system, and also known in the art.